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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,145	02/20/2002	Sang Hyeon Baeg	CISCO-4979	9291

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THELEN REID & PRIEST LLP  
CISCO  
P.O. BOX 640640  
SAN JOSE, CA 95164-0640

EXAMINER

TRIMMINGS, JOHN P

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/080,145	Applicant(s) BAEG ET AL.	
	Examiner John P. Trimmings	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 June 2005.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 and 14-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12, 14-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

*PD*

### **DETAILED ACTION**

This Office Action is in response to the applicant's amendment and RCE dated 6/6/2005.

The applicant amended claims 1, 11, 20 and 21.

The applicant canceled claim 12 in a prior amendment.

Claims 1-12 and 14-21 are pending.

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/6/2005 has been entered.

### ***Response to Arguments***

2. Applicant's arguments with respect to claims 1-12 and 14-21 have been considered but are moot in view of the new grounds of rejection (see below).

### ***Claim Rejections - 35 USC § 103***

3. Claims 1, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al., U.S. Patent No. 6763486, in view of Haulin, U.S. Patent No. 5996102.

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As per Claim 1:

Lai et al. teaches a receiver for boundary scan testing of differential interconnections between the receiver and a transmitter (column 1 lines 52-65 and column 7 lines 19-22), the receiver comprising: an input test buffer having null detection capability (column 6 lines 13-25); and an interface mechanism for providing at least partial test coverage for at least one of five fault syndromes that may be encountered during boundary scan testing (FIG.6 Frequency Detector Data). But Lai et al. fails to disclose the input test buffer having a common mode reference voltage. But in the analogous art of Haulin, testing is performed with the input test buffer having a common mode reference voltage (see FIG.2 where the buffer 96 is connected via 116 to common mode reference 108). And column 2 lines 43-50 and column 3 lines 14-18 relate the advantage being an improved method of testing differential circuits at high frequencies. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to apply Haulin's method of high speed test, including testing of common-mode sensitivity, to the test system of Lai et al. in order to improve testing at high frequencies.

As per Claims 20 and 21:

Lai et al. teaches a method and means for providing at least partial test coverage for at least one of five fault syndromes that may be encountered during boundary scan testing of differential interconnections between a receiver and a transmitter (column 1 lines 52-65 and column 7 lines 19-22), the method and means comprising: receiving an analog differential test signal pair (FIG.10 Rx, Aux1, Aux2);

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converting the analog differential test signal pair into a digital differential test signal pair (FIG.10 Boundary Decoder); and detecting a null condition in the digital differential test signal pair indicating that one of the five fault syndromes has occurred (column 6 lines 13-25). But Lai et al. fails to disclose the detecting utilizing a common mode reference voltage. But in the analogous art of Haulin, testing is performed with the input test buffer having a common mode reference voltage (see FIG.2 where the buffer 96 is connected via 116 to common mode reference 108). And in view of the motivation previously stated, the claims are rejected.

4. Claims 2-6, 8, 11, 12, 14, 15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al., U.S. Patent No. 6763486, in view of Kim et al., "Frequency Detection-Based Boundary-Scan Testing of AC Coupled Nets", and further in view of Haulin, U.S. Patent No. 5996102.

As per Claims 2 and 11:

Lai et al. further teaches the receiver as defined in claim 1, wherein the interface mechanism comprises a plurality of detectors (phase and frequency, see SUMMARY). However, Lai et al. fails to teach generating data and fault indicator signals. However, in an analogous art, Kim et al. does teach this feature in Table 1. And an advantage stated is that the approach is scalable with frequency and capacitor sizes. And one with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to provide the capabilities of Kim et al. with the receiver described by Lai et al. in order to provide multiple fault indicators. But neither Lai et al. nor Kim et al. teach the

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input test buffer utilizing a common mode reference voltage. But in the analogous art of Haulin, testing is performed with the input test buffer having a common mode reference voltage (see FIG.2 where the buffer 96 is connected via 116 to common mode reference 108). And in view of the motivation previously stated for Haulin, the claims are rejected.

As per Claims 3 and 12:

Lai et al. further teaches the receiver as defined in claim 2 or 11, wherein the interface mechanism further comprises a technology mapper (FIG.6 Frequency Detector) for processing the one or more output signals from the input test buffer (FIG.6 Rx Buffer) into one or more suitable input signals for the interface mechanism (FIG.6 Data). And in view of the motivation previously stated, the claims are rejected.

As per Claim 4:

Lai et al. further teaches the receiver as defined in claim 2, wherein the interface mechanism further comprises an integrator for processing the data and fault indicator signals of the detectors into one or more suitable output signals for the interface mechanism (FIG.10 Scan chain bit). And in view of the motivation previously stated, the claim is rejected.

As per Claims 5 and 14:

Kim et al. further teaches the receiver as defined in claim 2 or 11, wherein one of the plurality of detectors is a signal recoverer for recovery of the test data signal from the transmitter (see page 51 Figure IC3 Capture circuits used for scan cell inputs). And in view of the motivation previously stated, the claims are rejected.

As per Claims 6, 8, 15 and 17:

Kim et al. further teaches the receiver as defined in claim 2 or 11, wherein one of the plurality of detectors is an AC short/null detector and AC detector (see AC Detector Table 1).

5. Claims 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al., U.S. Patent No. 6763486, in view of Kim et al., "Frequency Detection-Based Boundary-Scan Testing of AC Coupled Nets", and in view of Haulin, U.S. Patent No. 5996102 as applied to Claim 2 or 11, and further in view of Ichie, U.S. Patent No. 5050187. Neither Kim et al., nor Lai et al., nor Haulin teach the receiver as defined in claim 2, wherein one of the plurality of detectors is a DC short detector. But in an analogous art, Ichie teaches this feature in FIG.11 F and in column 10 lines 41-63. And in column 1 lines 32-67 and column 2 lines 1-65 the inventor boasts of a system that detects and compensates for detrimental DC oriented transmission characteristics in an AC coupled system. And so, motivated as suggested to make a more reliable AC coupled system, one with ordinary skill in the art at the time of the invention would find it obvious to include the circuits of Ichie in the receiver of Kim et al. and Lai et al.

6. Claims 9, 10, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al., U.S. Patent No. 6763486, in view of Kim et al., "Frequency Detection-Based Boundary-Scan Testing of AC Coupled Nets", and in view of Haulin, U.S. Patent No. 5996102 as applied to claim 2 or 11, and further in view of Koenemann

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et al., U.S. Patent No. 5617426. The claims cite the receiver as defined in claim 2, wherein a heterogeneous capacitor detector comprises a first flip-flop for sampling a first signal on an even test clock signal, a second flip-flop for sampling a second signal on an odd test clock signal, and a logic gate for combining the outputs of the first and second flip-flops. Neither Lai et al., Kim et al., nor Haulin teach this feature. But in an analogous art, Koenemann et al. does teach a path delay fault detector (column 2 lines 47-51) which consists of 1<sup>st</sup> and 2<sup>nd</sup> flip-flops (FIG.5A 32, 33) and logic combining the outputs (FIG.5A 35). One with ordinary skill in the art at the time of the invention would recognize that capacitance in a line and path delays are synonymous. And in column 2 lines 11-52 the advantage is that such a circuit can detect delay faults. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to combine the latches of Koenemann et al. with the receiver of Kim et al. and Lai et al. in order to detect capacitance faults.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

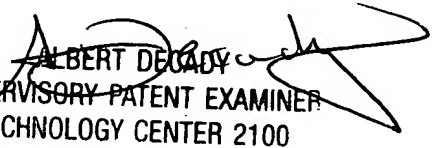
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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John P Trimmings  
Examiner  
Art Unit 2133

jpt



ALBERT DECADY  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100